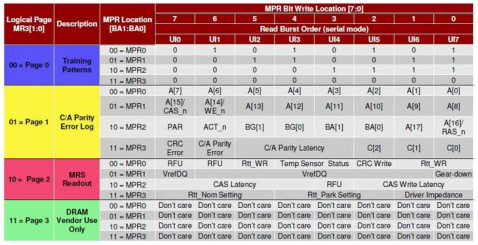
事例2：実機評価

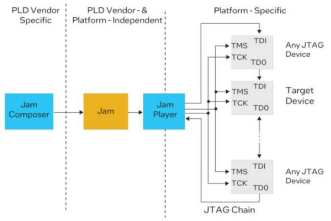
TDIPS

依頼内容	実施内容	成果物
実機動作観測	デバイス製品の実使用の動作観測を実施 CPUがドライブする入力波形、動作シーケンスの動作範囲、出力波形のマージン確認 実使用での不具合が発生しない事の妥当性の確認	動作波形 動作確認報告書

1.デバイス仕様

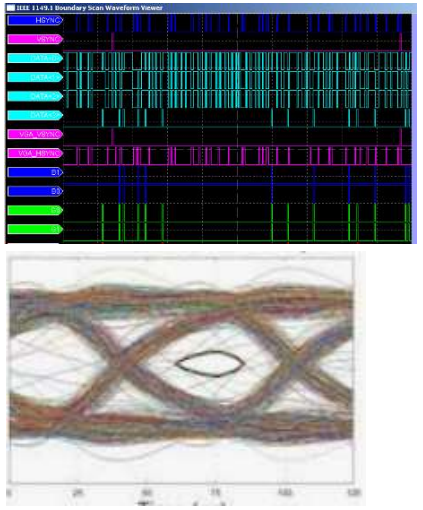


Logical Page MR3[1:0]	Description	MPR Location [BA1:BA0]	MPR Bit Write Location [7:0]							
			7	6	5	4	3	2	1	0
			Read Burst Order (serial mode)							
			UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
00 = Page 0	Training Patterns	00 = MPR0	0	1	0	1	0	1	0	1
		01 = MPR1	0	0	1	1	0	0	1	1
		10 = MPR2	0	0	0	0	1	1	1	1
		11 = MPR3	0	0	0	0	0	0	0	0
01 = Page 1	C/A Parity Error Log	00 = MPR0	A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]
		01 = MPR1	A[15]/ CAS_n	A[14]/ WE_n	A[13]	A[12]	A[11]	A[10]	A[9]	A[8]
		10 = MPR2	PAR	ACT_n	BG[1]	BG[0]	BA[1]	BA[0]	A[17]	A[16]/ RAS_n
		11 = MPR3	CRC Error	C/A Parity Error	C/A Parity Latency			C[2]	C[1]	C[0]
10 = Page 2	MRS Readout	00 = MPR0	RFU	RFU	Rtt_WR	Temp Sensor Status		CRC Write	Rtt_WR	
		01 = MPR1	VrefDQ	VrefDQ					Gear-down	
		10 = MPR2	CAS Latency			RFU		CAS Write Latency		
		11 = MPR3	Rtt_Nom Setting			Rtt_Park Setting		Driver Impedance		
11 = Page 3	DRAM Vendor Use Only	00 = MPR0	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care
		01 = MPR1	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care
		10 = MPR2	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care
		11 = MPR3	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care



2.機器接続

3.動作観測



実使用の状況で動作仕様の確認
（仕様通りの動作であるか確認）

フロー

デバイス仕様(設計仕様) → 機器接続 (ロジックアナライザ、オシロスコープ等) → 動作観測